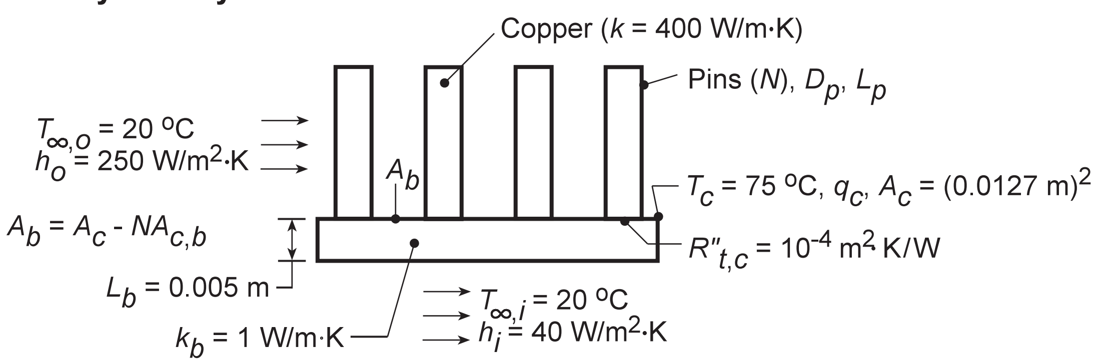
## PROBLEM 3.148

**KNOWN:** Geometry of pin fin array used as heat sink for a computer chip. Array convection and chip substrate conditions.

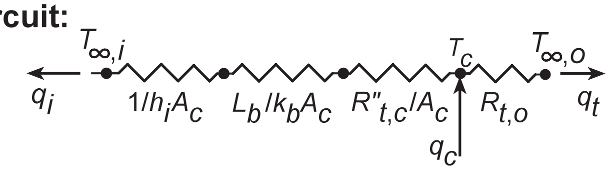
**FIND:** Effect of pin diameter, spacing and length on maximum allowable chip power dissipation.

**SCHEMATIC:**

**Physical System:**




**Thermal Circuit:**




**ASSUMPTIONS:** (1) Steady-state conditions, (2) One-dimensional heat transfer in chip-board assembly, (3) Negligible pin-chip contact resistance, (4) Constant properties, (5) Negligible chip thermal resistance, (6) Uniform chip temperature.

**ANALYSIS:** The total power dissipation is $q_c = q_i + q_t$, where

$$q_i = \frac{T_c - T_{\infty,i}}{\left(1/h_i + R''_{t,c} + L_b/k_b\right)/A_c} = 0.3\text{W}$$

and

$$q_t = \frac{T_c - T_{\infty,o}}{R_{t,o}}$$

The resistance of the pin array is

$$R_{t,o} = \left(\eta_o h_o A_t\right)^{-1}$$

where

$$\eta_o = 1 - \frac{NA_f}{A_t}\left(1 - \eta_f\right)$$

$$A_t = NA_f + A_b$$

$$A_f = \pi D_p L_c = \pi D_p \left(L_p + D_p/4\right)$$

Subject to the constraint that $N^{1/2}D_p \le 9$ mm, the foregoing expressions may be used to compute $q_t$ as a function of $D_p$ for $L_p = 15$ mm and values of N = 16, 25 and 36. Using the IHT *Performance Calculation, Extended Surface Model* for the *Pin Fin Array*, we obtain

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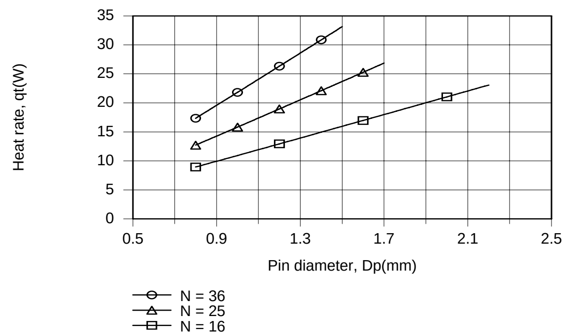
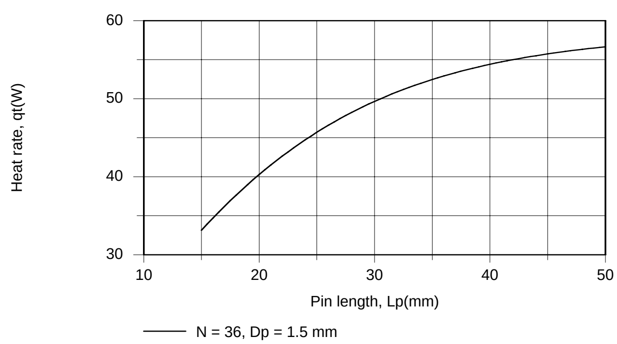
# PROBLEM 3.148 (Cont.)




Clearly, it is desirable to maximize the number of pins and the pin diameter, so long as flow passages are not constricted to the point of requiring an excessive pressure drop to maintain the prescribed convection coefficient. The maximum heat rate for the fin array ($q_t$ = 33.1 W) corresponds to N = 36 and $D_p$ = 1.5 mm. Further improvement could be obtained by using N = 49 pins of diameter $D_p$ = 1.286 mm, which yield $q_t$ = 37.7 W.

Exploring the effect of $L_p$ for N = 36 and $D_p$ = 1.5 mm, we obtain




Clearly, there are benefits to increasing $L_p$, although the effect diminishes due to an attendant reduction in $\eta_f$ (from $\eta_f$ = 0.887 for $L_p$ = 15 mm to $\eta_f$ = 0.471 for $L_p$ = 50 mm). Although a heat dissipation rate of $q_t$ = 56.7 W is obtained for $L_p$ = 50 mm, package volume constraints could preclude such a large fin length.

**COMMENTS:** By increasing N, $D_p$ and/or $L_p$, the total surface area of the array, $A_t$, is increased, thereby reducing the array thermal resistance, $R_{t,o}$. The effects of $D_p$ and N are shown for $L_p$ = 15 mm.