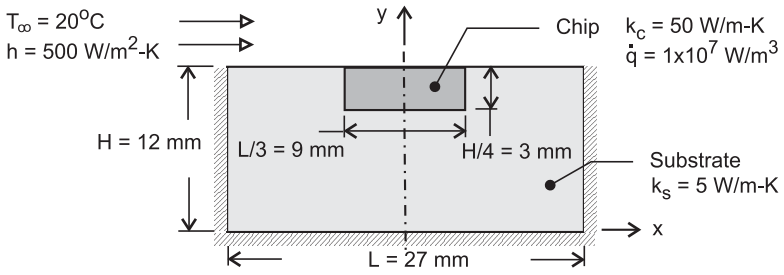
PROBLEM 4.96

KNOWN: Silicon chip mounted in a dielectric substrate. One surface of system is convectively cooled, while the remaining surfaces are well insulated. See Problem 4.93. Use the finite-element software *FEHT* as your analysis tool.

FIND: (a) The temperature distribution in the substrate-chip system; does the maximum temperature exceed 85°C?; (b) Volumetric heating rate that will result in a maximum temperature of 85°C; and (c) Effect of reducing thickness of substrate from 12 to 6 mm, keeping all other dimensions unchanged with $\dot{q} = 1\times10^7$ W/m^3; maximum temperature in the system for these conditions, and fraction of the power generated within the chip removed by convection directly from the chip surface.

SCHEMATIC:



ASSUMPTIONS: (1) Steady-state conditions, (2) Two-dimensional conduction in system, and (3) Uniform convection coefficient over upper surface.

ANALYSIS: Using *FEHT*, the symmetrical section is represented in the workspace as two connected regions, chip and substrate. *Draw* first the chip outline; *Specify* the material and generation parameters. Now, *Draw* the outline of the substrate, connecting the nodes of the interfacing surfaces; *Specify* the material parameters for this region. Finally, *Assign* the *Boundary Conditions*: zero heat flux for the symmetry and insulated surfaces, and convection for the upper surface. Draw *Element Lines*, making the triangular elements near the chip and surface smaller than near the lower insulated boundary as shown in a copy of the *FEHT* screen on the next page. Use the *Draw*|*Reduce M*esh command and *Run* the model.

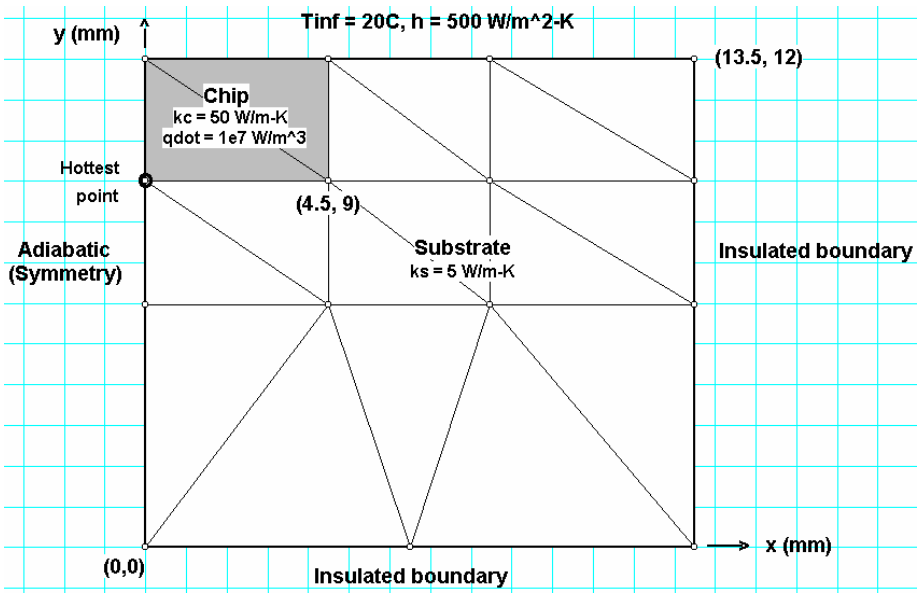
(a) Use the *View*|*Temperature* command to see the nodal temperatures through out the system. As expected, the hottest location is on the centerline of the chip at the bottom surface. At this location, the temperature is

$$T(0, 9\text{ mm}) = 46.7°C \quad <$$

(b) Run the model again, with different values of the generation rate until the temperature at this location is T(0, 9 mm) = 85°C, finding

$$\dot{q} = 2.43\times10^7\ \text{W/m}^3 \quad <$$

Continued …



(c) Returning to the model code with the conditions of part (a), reposition the nodes on the lower boundary, as well as the intermediate ones, to represent a substrate that is of 6-mm, rather than 12-mm thickness. Find the maximum temperature as

$$T(0,3\ \text{mm}) = 47.5°\text{C} \qquad <$$

Using the *View*|*Heat Flow* command, click on the adjacent line segments forming the chip surface exposed to the convection process. The heat rate per unit width (normal to the page) is

$$q'_{\text{chip,cv}} = 60.26\ \text{W/m}$$

The total heat generated within the chip is

$$q'_{\text{tot}} = \dot{q}(L/6 \times H/4) = 1\times10^{7}\ \text{W/m}^3 \times (0.0045\times0.003)\,\text{m}^2 = 135\ \text{W/m}$$

so that the fraction of the power dissipated by the chip that is convected directly to the coolant stream is

$$F = q'_{\text{chip,cv}} / q'_{\text{tot}} = 60.26/135 = 45\% \qquad <$$

COMMENTS: (1) Comparing the maximum temperatures for the system with the 12-mm and 6-mm thickness substrates, note that the effect of halving the substrate thickness is to raise the maximum temperature by less than 1°C. The thicker substrate does not provide significantly improved heat removal capability.

(2) Without running the code for part (b), estimate the magnitude of $\dot{q}$ that would make T(0, 9 mm) = 85°C. Did you get $\dot{q} = 2.43\times10^{7}$ W/m^3? Why?