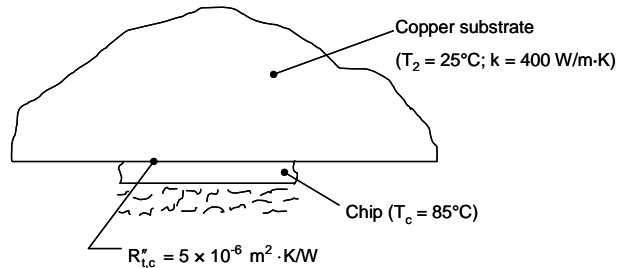


PROBLEM 4.34

KNOWN: Chip dimensions, contact resistance and substrate material.

FIND: Maximum allowable chip power dissipation.

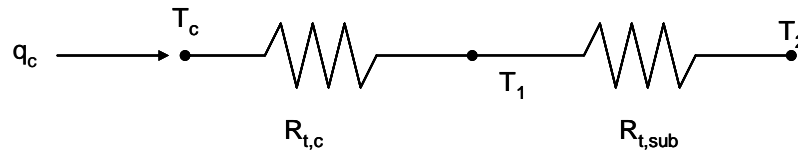
SCHEMATIC:



ASSUMPTIONS: (1) Steady-state conditions, (2) Constant properties, (3) Negligible heat transfer from back of chip, (4) Uniform chip temperature, (5) Infinitely large substrate, (6) Negligible heat loss from the exposed surface of the substrate.

PROPERTIES: Table A.1, copper (25 °C): $k = 400 \text{ W/m}\cdot\text{K}$.

ANALYSIS: For the prescribed system, a thermal circuit may be drawn so that



where T_1 is the temperature of the substrate adjacent to the top of the chip. For an infinitely thin square object in an infinite medium we may apply Case 14 of Table 4.1 ($q_{ss}^* = 0.932$) resulting in

$$q = q_{ss}^* k A_s (T_1 - T_2) / L_c$$

where $L_c = (A_s / 4\pi)^{1/2}$; $A_s = 2W_c^2$

Recognizing that the bottom surfaces of the chip and substrate are insulated, the heat loss to the substrate may be determined by combining the preceding equations and dividing by 2 (to account for no heat losses from the bottom of the chip) resulting in

$$q = (2\pi)^{1/2} q_{ss}^* W_c k (T_1 - T_2) = \frac{1}{R_{t,sub}} (T_1 - T_2)$$

$$\text{or} \quad R_{t,sub} = \frac{1}{(2\pi)^{1/2} \times 0.932 \times 0.016 \text{ m} \times 400 \text{ W/m}\cdot\text{K}} = 0.067 \text{ K/W}$$

The thermal contact resistance is

Continued...

PROBLEM 4.34 (Cont.)

$$R_{t,c} = \frac{R''_{t,c}}{W_c^2} = \frac{5 \times 10^{-6} \text{ m}^2 \cdot \text{K/W}}{(0.016 \text{ m})^2} = 0.0195 \text{ K/W}$$

Therefore, the maximum allowable heat dissipation is

$$q_c = \frac{(85 - 25)^\circ\text{C}}{(0.0195 + 0.067) \text{ K/W}} = 694 \text{ W} \quad <$$

COMMENTS: (1) The copper block provides $694/276 = 2.5$ times greater allowable heat dissipation relative to the heat sink of Problem 3.150. (2) Use of a large substrate would not be practical in many applications due to its size and weight. (3) The actual allowable heat dissipation is greater than calculated here because of additional heat losses from the bottom of the block and chip that are not accounted for in the solution.