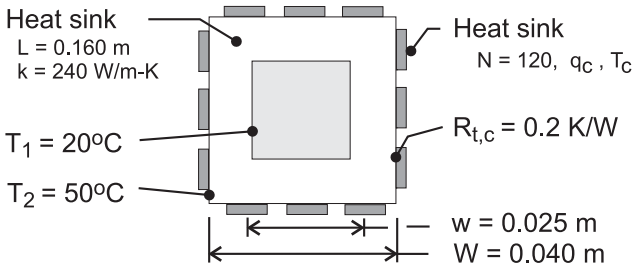
PROBLEM 4.28

KNOWN: Dimensions and surface temperatures of a square channel. Number of chips mounted on outer surface and chip thermal contact resistance.

FIND: Heat dissipation per chip and chip temperature.

SCHEMATIC:



ASSUMPTIONS: (1) Steady state, (2) Approximately uniform channel inner and outer surface temperatures, (3) Two-dimensional conduction through channel wall (negligible end-wall effects), (4) Constant thermal conductivity.

ANALYSIS: The total heat rate is determined by the two-dimensional conduction resistance of the channel wall, $q = (T_2 - T_1)/R_{t,cond(2D)}$, with the resistance determined by using Equation 4.21 with Case 11 of Table 4.1. For W/w = 1.6 > 1.4

$$R_{t,cond(2D)} = \frac{0.930\ \ln(W/w) - 0.050}{2\pi\ L\ k} = \frac{0.387}{2\pi(0.160\text{m})\,240\ \text{W/m}\cdot\text{K}} = 0.00160\ \text{K/W}$$

The heat rate per chip is then

$$q_c = \frac{T_2 - T_1}{N\ R_{t,cond(2D)}} = \frac{(50-20)°\text{C}}{120(0.0016\ \text{K/W})} = 156.3\ \text{W} \quad <$$

and, with $q_c = (T_c - T_2)/R_{t,c}$, the chip temperature is

$$T_c = T_2 + R_{t,c}\ q_c = 50°\text{C} + (0.2\ \text{K/W})156.3\ \text{W} = 81.3°\text{C} \quad <$$

COMMENTS: (1) By acting to *spread* heat flow lines away from a chip, the channel wall provides an excellent *heat sink* for dissipating heat generated by the chip. However, recognize that, in practice, there will be temperature variations on the inner and outer surfaces of the channel, and if the prescribed values of T_1 and T_2 represent minimum and maximum inner and outer surface temperatures, respectively, the rate is overestimated by the foregoing analysis. (2) The shape factor may also be determined by combining the expression for a plane wall with the result of Case 8 (Table 4.1). With S = [4(wL)/((W-w)/2)] + 4(0.54 L) = 2.479 m, $R_{t,cond(2D)} = 1/(Sk) = 0.00168$ K/W.